Analysis of Factors that Affect Yield in SMT Assembly

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1.0 Introduction

In many SMT production lines in operation today there is a substantial amount of data collection on yield and on the performance of the equipment in the line. Although a great deal of data is available, there is a lack of effective techniques for processing the data to determine the operational status of the equipment, or to be able to carry out predictive maintenance. Standard SPC charts represent the state-of-the-art in industry. However, the data collected from a standard SMT process is typically very noisy due to the natural variability of the SMT process itself, as well as the inherent measurement errors of the process monitoring equipment. To compound the problem, the relationships between all the various process variables and yield are unclear.

An on-going research effort at Georgia Tech is focused on the development of a novel probabilistic-based approach to the analysis of various factors that affect quality and yield in surface mount assembly lines. Our goal is to develop a robust methodology for detecting and identifying emerging problems in SMT assembly line operations with a view to being able to identify and ultimately correct those problems before they adversely affect production. The specific goal of the first phase of the research is to be able to determine appropriate operating ranges for the equipment in an SMT line, and to be able to use board-to-board measurements of solder print quality, placement accuracy, and yield after reflow to determine the operational status of that equipment.

Our overall approach to this challenging problem is based on the concept of a probabilistic network that defines the cause and effect relationships between equipment states and measured quantities relating to solder print quality, placement accuracy, and yield. The general form of a probabilistic network for an SMT line is shown in Figure 1. The upper circles (called nodes) in the network represent the states of the equipment in the line and the lower nodes represent quantities that

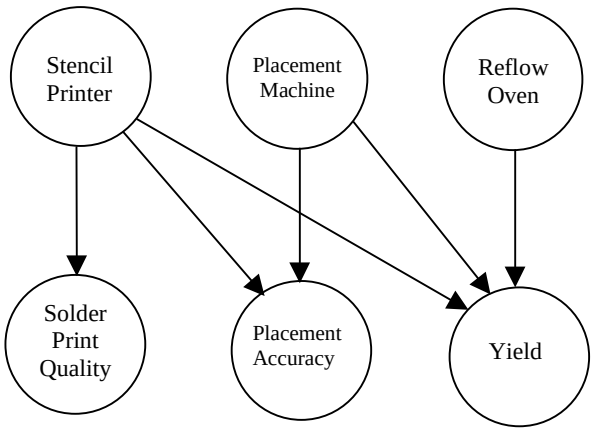

Figure 1. General probabilistic network for an SMT line

can be measured. The arrows in the network represent the cause and effect relationships; for example, the stencil printer affects the solder print quality, placement accuracy, and yield.

For the network given in Figure 1, the goal is to be able to deduce the states of the equipment based on measurements relating to solder print quality, placement accuracy, and yield. The determination of equipment states requires that various conditional probabilities be obtained a priori (before the line is in operation). In particular, it is necessary to know what effect equipment fault states have on solder print quality, placement accuracy, and yield. This can be accomplished by taking measurements while the equipment is operated in various possible fault states. At the time of writing this paper, we were able to consider only the effect on yield resulting from an intentional offset (fault) programmed into the placement machines. This corresponds to a calibration fault in the placement machines. In addition to the results given below involving the effect of placement offset errors, by the time of the conference we expect to also have results on the effect of solder paste deposition errors resulting from an intentional variation of machine parameters.

2.0 Experimental Setup

The experiments were carried out on the SMT line located in the Center for Board Assembly Research at the Georgia Tech Manufacturing Research Center. A schematic diagram of the line is shown in Figure 2.

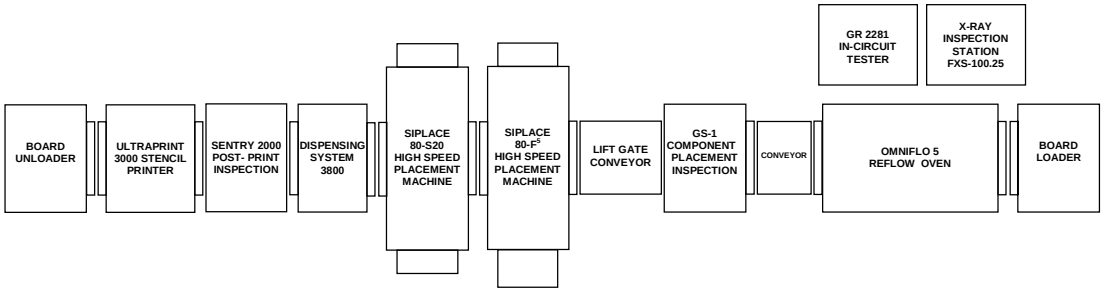

Figure 2. Georgia Tech SMT Assembly Line.

The equipment used for the yield analysis is listed below:

- MPM Ultraprint 3000 screen printer
- Cyberoptics Sentry 2000 post-print inspection tool
- Siemens SIPLACE S20 and F^5 placement machines
- MV Technology GS-1 post-placement inspection tool
- Electrovert OmniFlo 5 reflow oven
- GenRad GR2281 in-circuit tester
- Feinfocus X-ray station

The Cyberoptics Sentry 2000 provides measurements of the height, area, and volume of the solder paste bricks deposited on the pads by the screen printer. The MVT GS-1 provides measurements of the X-offset, Y-offset, and Θ-offset (skewness) of the components placed on the boards by the placement machines. A special printed circuit wiring board with the layout shown in Figure 3 was designed and manufactured for the experiments. The board was designed to provide a good cross section

of components typical of an actual state-of-the-art surface mount design. Enough test points were designed into the board so that every individual component on the board could be tested for open or short circuits after reflow using the GenRad GR2281 in-circuit tester. The component package types mounted onto each board were as follows:

- Passives: 0201, 0402, 0603, 0805, 1206, Micromelf 0805
- Integrated Circuits: BGA256, LQFP80, TSOP20/24

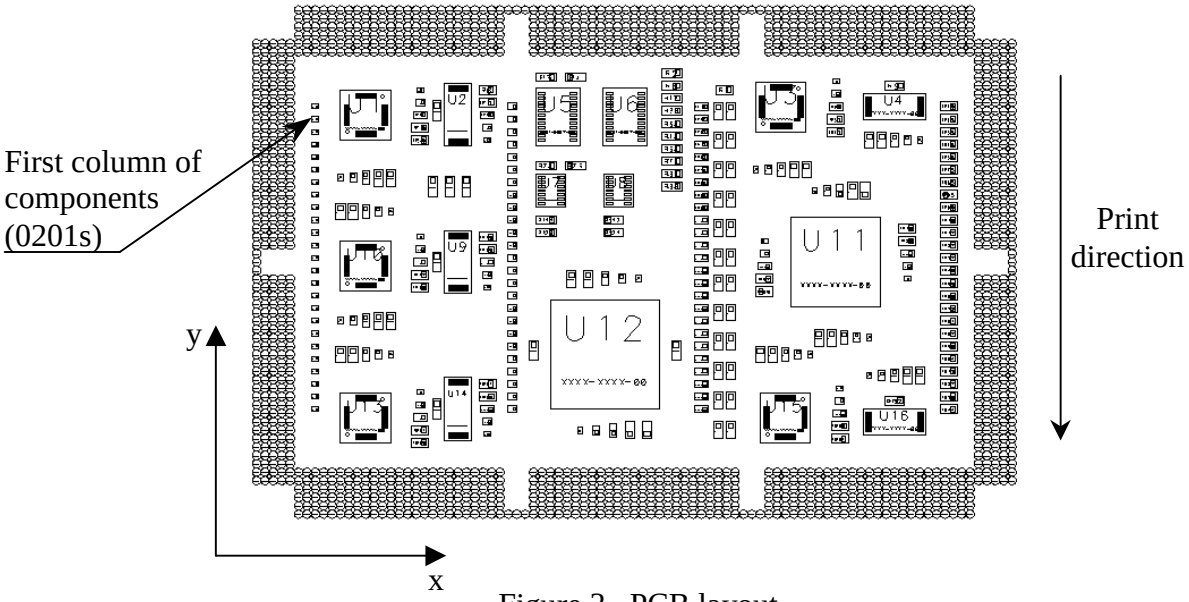

Figure 3. PCB layout

The dimensions of these component packages and the number placed on each board are given in Table 1. The passive components are placed onto the boards in columns with 0201s in the first column on the left-hand side of the board. As seen from Figure 3, there are also groupings of the passive components that are located throughout the board.

The smallest passive components are the 0201s, which are 20 mils by 10 mils in size. In the experiments, the 0201s were capacitors with a value of 3.8pF. We were not able to identify an electronics manufacturer that currently places 0201 components, and thus placing them provided an opportunity to study the next step in the reduction of discrete passive component dimensions in SMT assembly. Siemens has developed a nozzle to accommodate the 0201 package, which was used on the SIPLACE F^5 machine to place these components.

All the other passive component packages had real resistance values so that they could be tested electrically. The ICs were dummy components with isolated pins in the case of the LQFPs, and with daisy-chained leads in the case of the TSOPs and BGAs. The ICs could be tested for the existence of opens or shorts between leads and pads or balls. Note that with a pitch of 0.4 mm, the LQFPs are fine-pitch devices.

Component Type	Dimensions (in)	Qty./ board
Capacitor Chip 0201	0.02 x 0.01	47
Resistor Chip 0402	0.04 x 0.02	47
Resistor Chip 0603	0.06 x 0.03	47
Resistor Chip 0805	0.08 x 0.05	47
Resistor Chip 1206	0.12 x 0.06	28
Micromelf Resistor 0805	1.10 x 2.20	47
	Pitch (mm)	
Ball Grid Array BGA256	1.27	1
Thin Small Outline Pack TSOP20/24	0.5	5
Low Profile Quad Flat Pack LQFP 80	0.4	5

Table 1. Components assembled onto boards.

3.0 Board Runs

The initial experiment consisted of a 30-board run with the boards produced in 5 batches with each batch consisting of 6 boards. Each board was populated with the components listed in Table 1, resulting in a total of 274 components placed onto a board. To study the effect of a fault in the placement process, an intentional offset error was programmed into the placement machines. As indicated in Table 2, the amount of the offset is equal to a percentage of the pad width. Only those passive components located in the columns on the boards were shifted (offset) in the X direction, while all the ICs were shifted the same amount in both the X and Y directions. Figure 4 illustrates the shift for an IC. The values of the shifts are given in Table 3.

Boards 1-6	0% of component's pad width
Boards 7-12	25% of component's pad width
Boards 13-18	35% of component's pad width
Boards 19-24	45% of component's pad width
Boards 25-30	55% of component's pad width

Table 2. Amount of offset error in the placement machines.

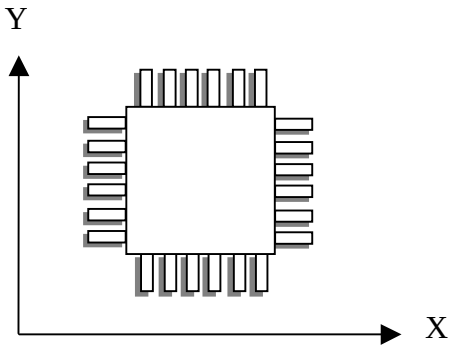

Figure 4. Shift in IC location.

Component	Pad width (mm)	25%	35%	45%	55%
LQFP80	0.254	0.0635	0.0889	0.1143	0.1397
TSOP20/24	0.3048	0.0762	0.10668	0.13716	0.16764
BGA256	0.762	0.1905	0.2667	0.3429	0.4191
0201	0.4064	0.1016	0.14224	0.18288	0.22352
0402	0.762	0.1905	0.2667	0.3429	0.4191
0603	1.143	0.28575	0.40005	0.51435	0.62865
0805	1.4224	0.3556	0.49784	0.64008	0.78232
1206	1.6256	0.4064	0.56896	0.73152	0.89408
MICROMELF 0805	1.270	0.3175	0.4445	0.5715	0.6985

Table 3. Values of the shifts.

4.0 Test Results

After all boards had completed the reflow process, the GenRad GR2281 in-circuit tester was used to inspect the PCBs for solder opens and shorts that may have been induced during PCB assembly. This section discusses the defects observed for both passive components and IC packages.

4.1 IC package defects

As noted in Table 1, each board contains 5 LQFPs (64 leads), 5 TSOPs (20 leads), and 1 BGA (256 balls). Table 4 lists the total number of defect opportunities (based on total leads) and defects encountered after the reflow process.

	Defect opportunities	Shorts	Opens
BGA	7680	0	2
LQFP	9600	19	0
TSOP	3000	0	0

Table 4. Defects for the ICs.

The data shown in Table 4 is not divided into batches due to the small number of defects that occurred. However, the 2 opens related to the BGA occurred on different boards in the 55% offset group (Batch 5). Also, 19 shorted pin pairs were encountered on the LQFPs. In addition, pins 3 and 4 of the U13s (see Figure 3) accounted for 12 of the 19 shorted pin pairs. The root cause for solder bridges occurring on the LQFPs is probably related to the screen printing process. This reason for the shorts becomes more likely after taking the LQFP's pitch (16 mils) into account. When the pitch is ≤ 16 mils, the solder paste printing process becomes far more critical due to the challenge of obtaining consistent paste deposition through the stencil apertures. Future experiments that vary screen printing parameters will probably induce more IC defects (i.e., opens and shorts).

4.2 Passive component defects

Defects encountered among the five varieties of SMT passive devices (0201, 0402, 0603, 0805, and 1206) were analyzed after the production run. This section only takes into account those passive

devices placed in columns on the PCB, resulting in 25 for each package type and providing a total of 125 defect opportunities per board. All defects were diagnosed as open circuits by the in-circuit test machine, and upon further inspection, can be classified in one of three categories: tombstoned, skewed, or missing/absent.

While all 0805 and 1206 devices were successfully placed, the 0402 and 0603 defects provided the most useful information for the process analysis. The plot in Figure 5 contains passive defect information and separates the 145 total defects into one of 5 batches (organized by placement machine offset percentage). Total defects for 0201, 0402, 0603 devices show an upward trend from 0% to 55% offset. However, 0201 defects were encountered during every batch, even at 0% offset. Only the 0402 and 0603 defects occurred with more consistency relative to increased offset. In the graph in Figure 6, note that the 0402 device process yield (~98%) is greater than the 0603 device process yield (86%). In addition, 0402 defects were not encountered until the 45% offset group.

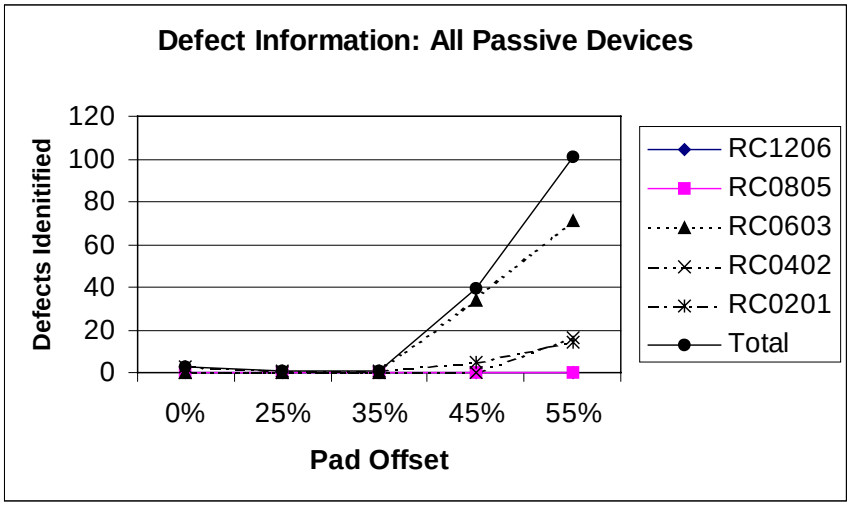

Figure 5. Number of opens as a function of offset.

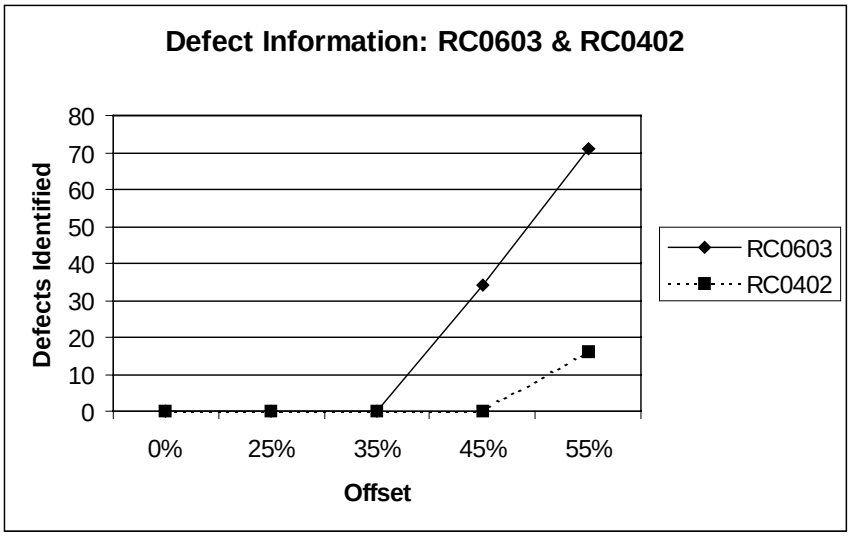

Figure 6. Defects for 0402 and 0603 components.

4.3 0201Components

Of the 47 0201 components on each board, 25 lie in the first column (starting from the left) of the PCB (Figure 3). The remaining 25 are organized in small groups containing an 0201, 0402, 0603, 0805, and Micromelf 0805. The PCB contains 22 of these groups, which are rotated either 0 or 90 degrees. As noted previously, placement offsets were varied (from 0 to 55% of the device's pad width) for the 0201 devices in the first column only. No offsets were introduced for the 0201s in the small groups.

The 30-board run produced 164 total defects diagnosed by the GenRad GR2281 in-circuit test system when all 47 0201 capacitors were inspected on every board (creating 1410 total defect opportunities and an 88% yield). After reviewing the in-circuit test (ICT) data, we observed that all identified defects were open-circuit related (i.e. open solder joint). Additional visual inspection determined that the defects can be further classified into the following categories: ~75% of the parts were tombstoned, 25% skewed, and <1% missing/absent. The graph in Figure 7 shows the breakdown of total defects with respect to each batch of 6 boards.

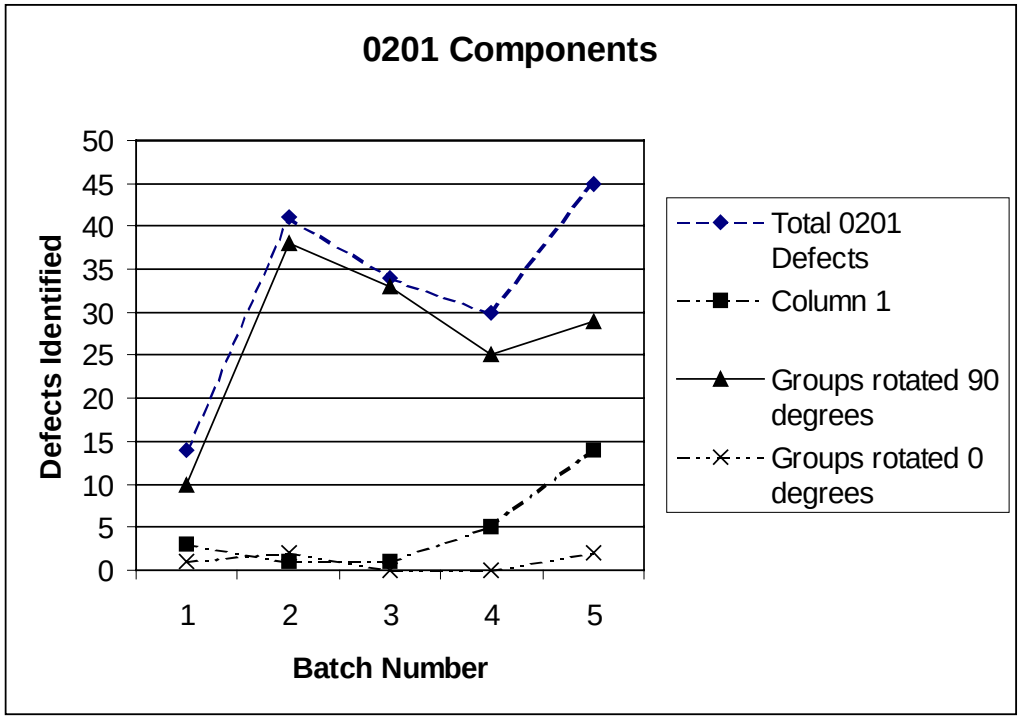

Figure 7. Defects for the 0201 components.

Since offsets were intentionally applied only to the 0201s in the first column, filtering out defects that occurred in the smaller groups and analyzing the defect data for the first column only provides another means of analysis. The first column contains 25 0201s which over the 30-board run, provide 750 total defect opportunities. After filtering the defect data for the 0201s in the first column only, the total number of defects equaled 24, producing a first pass yield of ~97%. An interesting observation is that only 4 of the defects in the column were classified as tombstoned parts while the remaining 20 resulted in skewed or mis-orientated parts. These defects appear to be evenly distributed across the first 4 batches. The fifth batch contains 14 of the 24 defects, and 8 of these 14 were observed in the final board of the batch of 30. In addition, we did observe an upward trend in defects occurring between boards 25

and 30 in the final batch, which may suggest that the process is gradually losing stability. We believe that the defects that occurred for the 0201s that were not offset were due primarily to the reflow process, but at the time of this writing we cannot confirm this.

In summary, the 0805 and 1206 devices all passed at ICT, the frequency of defects per board increased as the offset increased for the 0402 and 0603 devices, and the 0201s displayed a reasonable defect pattern for the components in the first column, but a sporadic defect pattern when all 47 devices were included.

5.0 Concluding Comments

We emphasize that the results discussed in this paper are very preliminary, especially given the relatively small sample size (i.e., the number of components placed). Due to the limited sample size, we did not attempt to compute defects in terms of parts per million (PPM), which is the standard unit used in industry. We also did not use measurements of the solder paste height, area, or volume after stencil printing, or measurements of offsets after component placement. We will use these measurements for the additional board runs that we have planned. The additional board runs should give us an adequate sample size, so that we should have reasonable confidence levels for the data. In addition to varying offsets in the placement machines, we have developed a design of experiments for varying other equipment parameters such as z-axis placement force, stencil printer parameters such as squeegee pressure and print speed, and reflow oven parameters such as conveyor speed and temperatures in the various zones. Using the data obtained from these runs, we expect to be able to determine a priori probabilities for solder print quality, placement accuracy, and yield given that the equipment is in the various possible fault states. These conditional probabilities can then be used with board-to-board measurement data to determine the states of the equipment during line operation. We expect to be able to present results on this at the conference.

6.0 Acknowledgements

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